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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/362,504
Filing Date: July 27, 1999
Appellant(s): RAVI ET AL.

Chung-Pok Leung
For Appellant

Supplemental EXAMINER'S ANSWER

This is in response to the appeal brief filed November 30, 2005 appealing from the Office action mailed April 28, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows: Claim 16 stands rejected under 35 USC 102(b), or in the alternative, under 35 USC 103(a).

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 4500408 A Boys; Donald R. et al. 2-1985

US 5319247 A	Matsuura; Masazumi	6-1994
US 5772771 A	Li; Shijian et al.	6-1998

Jin Onuki et al, "High-reliability interconnection formation by a two-step switching bias sputtering process", Thin Solid Films, January, 1995, pp. 182-188.

(9) Grounds of Rejection[1]

Claim Rejections - 35 USC § 102/103

Claim 16 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Jin Onuki et al[2]. Onuki teaches an integrated circuit (Figure 4; "LSIs" - Large Scale Interconnections; Abstract, Section 1) formed on a semiconductor substrate (Figure 4; "Si wafers" , Section 2.1) (Figure 4; "Si wafers" , Section 2.1) by the method of:

a. flowing a process gas (Argon, Section 2.1) into a substrate (Figure 4; "Si wafers" , Section 2.1) processing chamber (inherent, "base pressure before sputtering was $2x10^{-7}$ Pa" Section 2.1);

b. forming a plasma (Figure 4, Section 3.1, last paragraph) from said process gas (Argon, Section 2.1) by coupling sputtering energy ("The sputtering power was 4 kW..., Section 2.1, Figure 1a) into said substrate (Figure 4; "Si wafers" , Section 2.1) processing chamber (inherent, "base pressure before sputtering was $2x10^{-7}$ Pa" Section 2.1)

c. thereafter, maintaining said plasma (Figure 4, Section 3.1, last paragraph) to deposit a first layer (any one of 18 cycles for depositing "Al-0.5wt.%Cu-1wt.%Si films", Section 2.1) of a film ("Al-0.5wt.%Cu-1wt.%Si films", Section 2.1) over said substrate (Figure 4;

[1] Reproduced, verbatim, from the Final Rejection of April 28, 2005.
[2] High-reliability interconnection formation by a two-step switching bias sputtering process. Jin Onuki, Masayasu Nihei, Masahiro Koizumi. *Thin Solid Film ("Al-0.5wt.%Cu-1wt.%Si films", Section 2.1)s*, Vol. 266 (1995), pp. 182-188.

"Si wafers" , Section 2.1) by sputtering without biasing (Left side - Figure 1a; Section 2.1) said plasma (Figure 4, Section 3.1, last paragraph) toward said substrate (Figure 4; "Si wafers" , Section 2.1); and

d. thereafter, maintaining said plasma (Figure 4, Section 3.1, last paragraph) by maintaining coupling of said sputtering energy ("The sputtering power was 4 kW..., Section 2.1, Figure 1a) into said substrate (Figure 4; "Si wafers" , Section 2.1) processing chamber (inherent, "base pressure before sputtering was $2x10^{-7}$ Pa" Section 2.1) and biasing (Right side, Figure 1a, Section 2.1) said plasma (Figure 4, Section 3.1, last paragraph) toward said substrate (Figure 4; "Si wafers" , Section 2.1) to deposit a second layer of said film ("Al-0.5wt.%Cu-1wt.%Si films", Section 2.1) over said first layer (any one of 18 cycles for depositing "Al-0.5wt.%Cu-1wt.%Si films", Section 2.1), as claimed by claim 16

It is not clear in Jin Onuki's Figure 1a and accompanying text that Onuki's conventional sputtering is one complete process, distinct processes, or is a process applied recursively. However, Jin Onuki's disclosure, taken as a whole, teaches that it would have been obvious to one of ordinary skill in the art to apply Jin Onuki's conventional sputtering recursively as shown in Onuki's Figure 1b.

Motivation for a person of ordinary skill in the art to apply Jin Onuki's conventional sputtering recursively as shown in Onuki's Figure 1b is for controlling the argon content in the deposited films as taught by Onuki (left column; Page 184).

Claims 17-19, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boys et al (USPat.4,500,408) in view of Jin Onuki et al[3]. Boys teaches a sputter coating apparatus (Figure 1; column 4; lines 1-54) including:

i. A substrate (14; Figure 1; column 6, lines 5-40) processing system comprising: a housing (16; Figure 1; column 6, lines 5-40) for forming a vacuum chamber (12; Figure 1; column 6, lines 5-40); a vacuum pump (41; Figure 1; column 8, lines 5-40) for evacuating said vacuum chamber (12; Figure 1; column 6, lines 5-40); a pedestal (14; Figure 1; column 6, lines 5-40 - "mounted by conventional means (not shown)"), located within said housing (16; Figure 1; column 6, lines 5-40), configured to hold a substrate (14; Figure 1; column 6, lines 5-40); a gas distribution system (31-34; Figure 1; column 8, lines 5-40) fluidly coupled to said vacuum chamber (12; Figure 1; column 6, lines 5-40); a plasma (abstract...column 4, lines 3-28) generation system for forming a plasma (abstract...column 4, lines 3-28) from process gas (originating from 31; Figure 1) within said vacuum chamber (12; Figure 1; column 6, lines 5-40) and for selectively biasing (column 7, lines 43-61) said plasma (abstract...column 4, lines 3-28) toward said substrate (14; Figure 1; column 6, lines 5-40); a controller (57,58; Figure 1; column 8, lines 43-54) for controlling said vacuum pump (41; Figure 1; column 8, lines 5-40), said gas distribution system (31-34; Figure 1; column 8, lines 5-40) and said plasma (abstract...column 4, lines 3-28) generation system; a memory (column 8, lines 54-69) coupled to Boy's controller (57,58; Figure 1; column 8, lines 43-54) and storing a program (column 8, lines 54-69) for directing the operation of Boy's system, Boy's

[3] High-reliability interconnection formation by a two-step switching bias sputtering process. Jin Onuki, Masayasu

program (column 8, lines 54-69) including a set of instructions for depositing a film by first, controlling Boy's gas distribution system (31-34; Figure 1; column 8, lines 5-40) to introduce Boy's process gas (originating from 31; Figure 1) into Boy's chamber (12; Figure 1; column 6, lines 5-40); second, controlling Boy's plasma (abstract...column 4, lines 3-28) generation system to form a plasma (abstract...column 4, lines 3-28) from Boy's process gas (originating from 31; Figure 1) by coupling sputtering energy (column 14, lines 23-30) into Boy's vacuum chamber (12; Figure 1; column 6, lines 5-40) and deposit a first layer (column 14, lines 23-35) of Boy's film over Boy's substrate (14; Figure 1; column 6, lines 5-40) – claim 17

ii. The substrate (14; Figure 1; column 6, lines 5-40) processing system (Figure 1) of claim 19 wherein said source of silicon contains silane, as claimed by claim 31 – Applicant's claim requirement that "said source of silicon contains silane" is an intended use claim requirement. Further, it has been held that claim language that simply specifies an intended use or field of use for the invention generally will not limit the scope of a claim (Walter , 618 F.2d at 769, 205 USPQ at 409; MPEP 2106). Additionally, in apparatus claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim (In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963); MPEP2111.02).

Nihei, Masahiro Koizumi. *Thin Solid Film ("Al-0.5wt.%Cu-1wt.%Si films", Section 2.1)s*, Vol. 266 (1995), pp. 182-188.

iii. A computer readable storage medium having program (column 8, lines 54-69) code embodied therein, said program (column 8, lines 54-69) code for controlling a substrate (14; Figure 1; column 6, lines 5-29) processing system (Figure 1; column 6, lines 5-29), wherein said substrate (14; Figure 1; column 6, lines 5-29) processing system (Figure 1; column 6, lines 5-29) includes a processing chamber (16; Figure 1; column 6, lines 5-29), a gas delivery system (31-34; Figure 1), a plasma generation system (Figure 1) and a controller (57,58; Figure 1; column 8, lines 43-54) configured to control the gas delivery system (31-34; Figure 1) and the plasma generation system (Figure 1) said program (column 8, lines 54-69) code controlling the semiconductor processing system (Figure 1; column 8; lines 54-69) to process a wafer in the chamber (16; Figure 1; column 6, lines 5-29) in accordance with the following:

a. a first set of computer instructions (column 8; lines 54-69) for controlling the gas delivery system (31-34; Figure 1) to introduce a process gas (originating from 31; Figure 1) into the processing chamber (16; Figure 1; column 6, lines 5-29);

b. a second set of computer instructions (column 8; lines 54-69) for controlling the plasma generation system (62, 63; Figure 1 - column 9; lines 27-46) to form a plasma (column 1, lines 20-40) from the process gas (originating from 31; Figure 1) by coupling sputtering ("sputtering rate and sputtering uniformity"; abstract) energy (column 14, lines 23-30) into said processing chamber (16; Figure 1; column 6, lines 5-29) to deposit a first layer (column 1, lines 42-50) of a film over a substrate (14; Figure 1; column 6, lines 5-29) – claim 32

Boys does not teach:

iv. by sputtering without biasing Boy's plasma (abstract...column 4, lines 3-28) towards Boy's substrate (14; Figure 1; column 6, lines 5-40); and third, controlling Boy's plasma (abstract...column 4, lines 3-28) generation system to maintain Boy's plasma (abstract...column 4, lines 3-28) by maintaining coupling of Boy's sputtering energy (column 14, lines 23-30) into Boy's vacuum chamber (12; Figure 1; column 6, lines 5-40) and bias Boy's plasma (abstract...column 4, lines 3-28) toward Boy's substrate (14; Figure 1; column 6, lines 5-40) to deposit a second layer of Boy's film over Boy's first layer (column 14, lines 23-35) – claim 17

v. The substrate (14; Figure 1; column 6, lines 5-40) processing system of claim 17 wherein Boy's program (column 8, lines 54-69) further includes instructions for depositing a plurality of Boy's first layers (column 14, lines 23-35) and Boy's second layers by fourth, depositing a third layer of Boy's film over Boy's second layer by controlling Boy's plasma (abstract...column 4, lines 3-28) generation system to maintain Boy's plasma (abstract...column 4, lines 3-28) by maintaining coupling of Boy's sputtering energy (column 14, lines 23-30) into Boy's vacuum chamber (12; Figure 1; column 6, lines 5-40) and stop biasing (column 7, lines 43-61) Boy's plasma (abstract...column 4, lines 3-28) toward Boy's substrate (14; Figure 1; column 6, lines 5-40); fifth, depositing a fourth layer of Boy's film over Boy's third layer by controlling Boy's plasma (abstract...column 4, lines 3-28) generation system to maintain Boy's plasma (abstract...column 4, lines 3-28) by maintaining coupling of Boy's sputtering energy (column 14, lines 23-30) into Boy's vacuum chamber (12; Figure 1; column 6, lines 5-40) and bias Boy's plasma (abstract...column 4, lines 3-28) toward Boy's substrate (14; Figure 1; column 6, lines 5-

40); and sixth, performing the second and third steps iteratively at least once until a desired thickness of Boy's film is reached – claim 18

vi. The apparatus of claim 17 wherein said gas distribution system (31-34; Figure 1; column 8, lines 5-40) includes sources of silicon and oxygen fluidly coupled to said gas distribution system (31-34; Figure 1; column 8, lines 5-40), as claimed by claim 19 – However, it has been held that claim language that simply specifies an intended use or field of use for the invention generally will not limit the scope of a claim (Walter , 618 F.2d at 769, 205 USPQ at 409; MPEP 2106). Additionally, in apparatus claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim (In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963); MPEP2111.02).

vii. depositing by sputtering ("sputtering rate and sputtering uniformity"; abstract) without biasing (column 7, lines 43-61) Boys' plasma (column 1, lines 20-40) towards Boys' substrate (14; Figure 1; column 6, lines 5-29); and

a. a third set of computer instructions for controlling Boys' plasma (column 1, lines 20-40) generation system (31-34; Figure 1) to maintain Boys' plasma (column 1, lines 20-40) by maintaining coupling of Boys' sputtering ("sputtering rate and sputtering uniformity"; abstract) energy (column 14, lines 23-30) into Boys' processing chamber (16; Figure 1; column 6, lines 5-29) and to bias Boys' plasma (column 1, lines 20-40) toward Boys' substrate (14; Figure 1; column 6, lines 5-

29) to deposit a second layer of Boys' film over Boys' first layer (column 1, lines 42-50) – claim 32

Jin Onuki et al is discussed above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made for Boys to use Jin Onuki's conventional sputtering method (Fig. 1(a)) as part of Boys' program (column 8, lines 54-69) for directing the operation of Boy's system by Boy's controller (57,58; Figure 1; column 8, lines 43-54).

Motivation for Boys to use Jin Onuki's conventional sputtering method (Fig. 1(a)) as part of Boys' program for directing the operation of Boy's system by Boy's controller is to deposit films for conventional "step coverage" and "electromigration resistance" as taught by Jin Onuki (abstract).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li, Shijian et al (USPat. 5,772,771 A) in view of Jin Onuki et al[4]. Li et al teaches:

i. A high-density plasma (column 1, lines 20-40) chemical vapor deposition system (Figure 1; column 3, lines 21-46) comprising:

   b. a housing (18; Figure 1; column 3, lines 49-65) for forming a vacuum chamber (18; Figure 1; column 3, lines 49-65); a pedestal (14; Figure 1; column 3, lines 49-65), located within said housing (18; Figure 1; column 3, lines 49-65), for holding a substrate (20; Figure 1; column 3, lines 49-65); means for introducing reactants (compare Applicant's 14; Figure 1 to Li's 34; Figure 1) into said vacuum chamber (18; Figure 1; column 3, lines 49-65); means for generating a

plasma (compare Applicant's elements 24, 26, and 44; Figure 1 to Li's 25, 8, and 14, respectively; Figure 1) from said reactants by applying a sputtering ("sputtering rate and sputtering uniformity"; abstract) power to said reactants to deposit a first layer (column 1, lines 42-50) of a film on said substrate (20; Figure 1; column 3, lines 49-65) during a first time period said first layer (column 1, lines 42-50) for the reduction of mechanical stress in a subsequently deposited layer of a silicon oxide film – claim 20. Applicant's claim requirement of "said first layer for the reduction of mechanical stress in a subsequently deposited layer of a silicon oxide film" is an intended use claim requirement. Further, it has been held that claim language that simply specifies an intended use or field of use for the invention generally will not limit the scope of a claim (Walter , 618 F.2d at 769, 205 USPQ at 409; MPEP 2106). Additionally, in apparatus claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim (In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963); MPEP2111.02).

Li does not teach:

viii. means for biasing (column 7, lines 43-61) Li's plasma (column 1, lines 20-40) toward Li's substrate (20; Figure 1; column 3, lines 49-65) during a second time period after Li's first time period to enhance a sputtering ("sputtering rate and sputtering uniformity";

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[4] High-reliability interconnection formation by a two-step switching bias sputtering process. Jin Onuki, Masayasu

abstract) of Li's plasma (column 1, lines 20-40) while maintaining application of Li's sputtering ("sputtering rate and sputtering uniformity"; abstract) power to Li's reactants and deposit Li's subsequent layer

Jin Onuki et al is discussed above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made for Li to use Jin Onuki's conventional sputtering method (Fig. 1(a)) as part of Li's control for directing the operation of Li's apparatus.

Motivation for Li to use Jin Onuki's conventional sputtering method (Fig. 1(a)) as part of Li's control for directing the operation of Li's apparatus is to deposit films for conventional "step coverage" and "electromigration resistance" as taught by Jin Onuki (abstract).

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li, Shijian et al (USPat. 5,77,2771 A) and Jin Onuki et al[5] in view of Boys et al (USPat.4,500,408). Li, Shijian et al and Jin et al are discussed above. Li, Shijian et al and Jin et al do not teach:

ix. The apparatus of claim 20, further comprising means for maintaining a pressure of between about 0.001-10 torr in said vacuum chamber (18; Figure 1; column 3, lines 49-65) while said films are deposited, as claimed by claim 21. Applicant's means for maintaining a pressure is supported in Applicant's page 6 – "A gas distribution system introduces a process gas containing reactants into the vacuum chamber and sets and maintains a selected pressure in the chamber along with a vacuum pump and valve system."

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x. The apparatus of claim 20, further comprising means for maintaining a wafer temperature of between about 100-500°C in said vacuum chamber while said film s are deposited, as claimed by claim 22

Boys et al teach equivalent pressure control means including a gas distribution system (31-34; Figure 1) introduces a process gas (31) containing reactants into the vacuum chamber (16) and sets and maintains a selected pressure (column 8; lines 7-13) in the chamber along with a vacuum pump (41) and valve system (32). Boys et al further teaches equivalent temperature control means (claim 20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for Li, Shijian et al and Jin Onuki et al to add Boys' pressure and temperature control means.

Motivation for Li, Shijian et al and Jin Onuki et al to add Boys' pressure and temperature control means is for controlling the processing during operation as taught by Boys (column 11; lines 14-58).

Claims 23, 24, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jin Onuki et al[6] in view of Matsura (USPat. 5,319,247). Jin Onuki teaches:

i. An integrated circuit (Figure 4; "LSIs" - Large Scale Interconnections; Abstract, Section 1) formed on a semiconductor substrate (Figure 4; "Si wafers" , Section 2.1), said integrated circuit (Figure 4; "LSIs" - Large Scale Interconnections; Abstract, Section 1) comprising: (a) a plurality of active devices (LSIs, Section 1) formed in said

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[6] High-reliability interconnection formation by a two-step switching bias sputtering process. Jin Onuki, Masayasu Nihei, Masahiro Koizumi. *Thin Solid Film ("Al-0.5wt.%Cu-1wt.%Si films", Section 2.1)s*, Vol. 266 (1995), pp. 182-188.

semiconductor substrate (Figure 4; "Si wafers" , Section 2.1); (b) at least one metal layer (Al; Figure 4) formed above said semiconductor substrate (Figure 4; "Si wafers" , Section 2.1); and (c) at least one insulating layer (SiO2; Figure 4) formed between said metal layer (Al; Figure 4) and said semiconductor substrate (Figure 4; "Si wafers" , Section 2.1), said insulating layer (SiO2; Figure 4) having a plurality of patterned holes (Figure 11) filled with electrically conductive material ("Al"; Figure 4) to electrically connect elected portions of said metal layer (Al; Figure 4) to selected portions of said semiconductor substrate (Figure 4; "Si wafers" , Section 2.1) - claim 23

ii. The integrated circuit (Figure 4; "LSIs" - Large Scale Interconnections; Abstract, Section 1) of claim 23, further comprising: (d) a second metal layer ("Al"; Figure 4(3)) formed above said semiconductor substrate (20; Figure 1; column 3, lines 49-65) - claim 24

iii. The integrated circuit (Figure 4; "LSIs" - Large Scale Interconnections; Abstract, Section 1) of claim 23 wherein the first silicon oxide layer (SiO2; Figure 4) is deposited on the substrate (Figure 4; "Si wafers" , Section 2.1) by placing the substrate in a process chamber (inherent, "base pressure before sputtering was $2x10^{-7}$ Pa" Section 2.1) applying a sputtering power ("The sputtering power was 4 kW..., Section 2.1, Figure 1a) to reactants to generate a plasma in the process chamber - claim 36

Jin Onuki does not teach:

i. wherein said insulating layer (SiO2; Figure 4) comprises a first silicon oxide layer and a second silicon oxide layer, said first and said second silicon oxide layers deposited using a high-density plasma chemical vapor deposition process, said first silicon oxide layer

deposited for the reduction of mechanical stress in said second silicon oxide layer – claim 23

ii. Jin Onuki's second metal layer ("Al"; Figure 4(3)) is below said at least one insulating layer (SiO2; Figure 4); (e) a second insulating layer (SiO2; Figure 4) formed between said second metal layer ("Al"; Figure 4(3)) and said semiconductor substrate (20; Figure 1; column 3, lines 49-65), said second insulating layer (SiO2; Figure 4) having a second plurality of patterned holes (Figure 11) filled with electrically conductive material ("Al"; Figure 4) to electrically connect selected portions of said second metal layer ("Al"; Figure 4(3)) to selected areas of said plurality of active devices (LSIs, Section 1), as claimed by 24

iii. A second silicon oxide layer is deposited on the first silicon oxide layer by biasing the plasma toward the substrate while maintaining application of the sputtering power to the reactants, as claimed by claim 36

Matsura teaches a method of forming silicon and oxygen combined thin films for "superior crack resistance and insulation" (silicate, column 6, lines 4-11) by optionally (embodiment) applying silane and oxygen gases (column 7, line 67; claim 1). Operating conditions of pressure: 1mTorr<=100mT<=10Torr (column 6, line 33) and temperature: 100°C <= 350°C <= 450°C <= 500°C (column 6, line 38) are specifically met by Matsuura.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform film depositions by sputtering cycles of conventional sputtering (Figure 1(a)) as taught by Jin Onuki thereby depositing plural silicon oxide layers.

Motivation to perform film depositions by sputtering cycles of conventional sputtering (Figure 1(a)) as taught by Jin Onuki thereby depositing plural silicon oxide layers is to deposit films of "superior crack resistance and insulation", as taught by Matsura (silicate, column 6, lines 4-11).

Claim 25-30, 33, 34, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boys et al (USPat.4,500,408) and Jin Onuki et al[7] in view of Li, Shijian et al (USPat. 5,772,771 A). Boys and Jin Onuki are discussed above. Boys and Jin Onuki do not teach plasma generation by an inductively coupled plasma.

Li teaches inductively coupled plasma generation (8; Figure 1). Li further teaches the inductively coupled plasma (8; Figure 1) is formed from process gas (originating from 70, 72; Figure 1) using only RF energy (10; Figure 1) applied to a coil (8; Figure 1) disposed about the processing chamber (18; Figure 1; column 3, lines 49-65), as claimed by claim 26, 33. Li further teaches the substrate (20; Figure 1; column 3, lines 49-65) processing system (Figure 1; column 3, lines 21-46) of claim 25 wherein said substrate (20; Figure 1; column 3, lines 49-65) processing chamber (18; Figure 1; column 3, lines 49-65) is a high-density plasma (column 1, lines 20-40) chemical vapor deposition chamber (18; Figure 1; column 3, lines 49-65) and said inductively coupled plasma (column 1, lines 20-40) is a high density plasma (column 1, lines 20-40), as claimed by claim 27, 34.

Li further teaches:

i. The processing system (Figure 1; column 3, lines 21-46) of claim 17 wherein said plasma (column 1, lines 20-40) generating system (Figure 1; column 3, lines 21-46) includes a first electrode (25; Figure 1), a second electrode (14; Figure 1), and a coil (8; Figure 1)

disposed about the vacuum chamber (18; Figure 1; column 3, lines 49-65), wherein said pedestal (14; Figure 1; column 3, lines 49-65) includes said second electrode (14; Figure 1), as claimed by claim 30

ii. The substrate (20; Figure 1; column 3, lines 49-65) processing system (Figure 1; column 3, lines 21-46) of claim 30 wherein the substrate (20; Figure 1; column 3, lines 49-65) is disposed on said second electrode (14; Figure 1) and electric energy (26, 22; Figure 1) is applied to said first and second electrodes while maintaining the application of said RF energy, as claimed by claim 28

iii. The substrate (20; Figure 1; column 3, lines 49-65) processing system (Figure 1; column 3, lines 21-46) of claim 17 wherein said process gas (originating from 31; Figure 1) introduced by said gas distribution system (Figure 1; column 3, lines 21-46) (31-34; Figure 1; column 8, lines 5-40) includes flows of silicon and Oxygen, as claimed by claim 29, 35 – Applicant's claim requirement that the "gas distribution system includes flows of silicon and Oxygen" is an intended use claim requirement. Further, it has been held that claim language that simply specifies an intended use or field of use for the invention generally will not limit the scope of a claim (Walter , 618 F.2d at 769, 205 USPQ at 409; MPEP 2106). Additionally, in apparatus claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim (In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963); MPEP2111.02).

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[7] High-reliability interconnection formation by a two-step switching bias sputtering process. Jin Onuki, Masayasu

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add Li's inductively coupled plasma generation (8; Figure 1) to Boys' and Jin Onuki's apparatus.

Motivation to add Li's inductively coupled plasma generation to Boys' and Jin Onuki's apparatus is for maintaining high density plasmas at taught by Li (column 1, lines 19-25).

(10) Response to Arguments

The sum-total of Applicant's arguments are centered on the Examiner's primary base reference to Jin Onuki et al. As cited in the Examiner's final rejection, Onuki's section 2, Figures 1(a) and 1(b) appear to either anticipate or make obvious Applicant's claimed inventions. Independent method claim 16 and independent apparatus claims 17, 20, and 32 all require steps taken, either by a controller/computer or in method form, that a first film(s) be deposited on a substrate by first applying sputtering energy and not biasing the substrate followed by maintaining sputtering energy and also biasing the substrate to deposit additional film(s).

Page 8 of the brief states:

"

Onuki et al, however, specifically discloses terminating the sputtering power during application of the bias voltage....

"

With regard to Onuki's Figure 1(a) and 1(b), the Examiner cited in the final rejection that "It is not clear in Jin Onuki's Figure 1a and accompanying text that Onuki's conventional sputtering is one complete process, distinct processes, or is a process applied recursively. However, Jin

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Nihei, Masahiro Koizumi. *Thin Solid Film ("Al-0.5wt.%Cu-1wt.%Si films", Section 2.1)s*, Vol. 266 (1995), pp. 182-

Onuki's disclosure, taken as a whole, teaches that it would have been obvious to one of ordinary skill in the art to apply Jin Onuki's conventional sputtering recursively as shown in Onuki's Figure 1b."

Onuki's Figure 1(a) teaches a "Conventional Sputtering" procedure. Onuki's Figure 1(a) has two boxes that appear to a "Conventional DC Sputtering" application and "Conventional DC Bias Sputtering" application. At first appearance, Onuki's Figure 1(a) appears to teach distinct processes, however, Onuki's Figure 1(b), immediately below Figure 1(a), shows, and the discussion supports (Section 2.1) one complete process where each box represents a processing *state that is repeated* over several times to deposit films discussed in section 2.1. Each of the boxes in Figure 1(b) switches sputtering on and off out of phase with a bias voltage. The Examiner thus believes that there is sufficient teaching in Onuki's Figure 1(a),(b) to suggest that Onuki's disclosure, taken as a whole, teaches that it would have been obvious to one of ordinary skill in the art to apply Jin Onuki's conventional sputtering recursively as shown in Onuki's Figure 1b. Clearly, Figure 1(a) can, at a glance, be quickly interpreted as a continuous process thus anticipating Applicant's invention, or at least, upon further reading of Onuki, be a process that can be conducted recursively (as suggested by Figure 1(b)) again meeting applicant's claimed invention as conveyed in the Examiner's final action.

Applicant further states on page 8:

"

Onuki et al clearly does not teach depositing two different layers.

"

188.

With respect to independent method claim 16 and independent apparatus claims 17, 20, and 32 that the reference fails to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "Onuki et al clearly does not teach depositing two different layers.") is not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Independent claims 16, 17, 20, and 32 do not distinguish on film identity in the distinct processing steps. In fact, independent claims 17, 20, and 32 are broad enough to read on a single film identity being deposited under different processing conditions. Claims 16, 17, 20, and 32 each only require a "first layer" and "second layer". Independent article claim 23 is rejected separately and does require film identities – "metal layer" and "insulating layer". Yet, with respect to claim 23, the Examiner cites Onuki as teaching at least one metal layer (Al; Figure 4) formed above said semiconductor substrate (Figure 4; "Si wafers" , Section 2.1); and at least one insulating layer (SiO2; Figure 4) formed between said metal layer (Al; Figure 4) and said semiconductor substrate (Figure 4; "Si wafers" , Section 2.1).

Applicant states, with respect to claim 23:

"

Nor does Jin Onuki et al recognize that the first layer formed without biasing the plasma is a reduced stress layer for reducing the stress of films deposited on the substrate.

" (page 8, bottom)

and

"

...Onuki et al does not teach or suggest two silicon oxide layers, wherein the first silicon oxide layer is deposited for the reduction of mechanical stress in the second silicon oxide layer.

" (page 14, top)

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In particular, the Examiner cites Matsura as teaching a method of forming silicon and oxygen combined thin films for "superior crack resistance and insulation" (silicate, column 6, lines 4-11) by optionally (embodiment) applying silane and oxygen gases (column 7, line 67; claim 1). Operating conditions of pressure: 1mTorr<=100mT<=10Torr (column 6, line 33) and temperature: 100°C <= 350°C <= 450°C <= 500°C (column 6, line 38) are specifically met by Matsuura.

With respect to claim 18, Applicant states:

"

In addition, claim 18 further recites that the program includes instructions for depositing a plurality of the first layers and second layers until the desired thickness of the film is reached. The references do not disclose or suggest depositing a plurality of first layers by sputtering without biasing the plasma and second layers by sputtering and biasing the plasma.

"

Claims 17-19, 31, and 32 were rejected under Boys et al (USPat.4,500,408) in view of Jin Onuki et al. Each reference is directed to sputtering methods. In particular, Boys teaches a memory (column 8, lines 54-69) coupled to Boy's controller (57,58; Figure 1; column 8, lines 43-54) and

storing a program (column 8, lines 54-69) for directing the operation of Boy's system, Boy's program (column 8, lines 54-69) including a set of instructions for depositing a film by first, controlling Boy's gas distribution system (31-34; Figure 1; column 8, lines 5-40) to... (see Final rejection).

Because of the Examiner's citation of Boys et al as teaching Applicant's claimed elements, the Examiner does not understand Applicant's position of "The Examiner recognizes that Boys et al does not teach a controller or a memory storing a program" (Page 11 of brief). The Examiner's final rejection is clear to the contrary.

Applicant states, with respect to claim 23:

"

...the Examiner alleges that "the sole difference between the claimed invention and the above conveyed prior art is the lack of intended use in Applicant's product claim."

"

The Examiner has not made this argument as part of his rejection of claims 23, 24, and 36. What the Examiner was intending to point out in the response to arguments section of the final rejection is that because Matsura teaches the same materials, then because the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent (In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977); MPEP 2112.01). The Examiner further pointed out, in his rejection of claims 23, 24, and 36, that Matsura teaches a method of forming silicon and oxygen combined thin films for "superior crack resistance and insulation" (silicate, column 6, lines 4-11) by optionally (embodiment) applying silane and oxygen gases (column 7, line 67; claim 1).

Applicant's state:

"

The claim features not taught or suggested in Onuki et al and Matsura are not merely intended use features.

"

In response, Applicants mis-state the Examiner's interpretation of apparatus features that the Examiner believes to be intended use. Nowhere in the rejection of article claims 23, 24, and 36 does the Examiner apply an intended use argument. See final rejection. Indeed *all elements* in article claims 23, 24, and 36 are fully accorded patentable weight. Only in Apparatus claims 17-22, and 25-31 does the Examiner apply intended use arguments directed to process gas and/or film identities. See the final rejection.

In response to applicant's argument (third paragraph, page 14) that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

With respect to Applicant's arguments with respect to claims 24 and 36, see last paragraph page 14, it was Jin Onuki was cited as teaching an integrated circuit (Figure 4; "LSIs" - Large Scale Interconnections; Abstract, Section 1) of claim 23, further comprising: (d) a second metal layer ("Al"; Figure 4(3)) formed above said semiconductor substrate (20; Figure 1; column 3, lines 49-

65) - claim 24. Onuki's integrated circuit (Figure 4; "LSIs" - Large Scale Interconnections; Abstract, Section 1) of claim 23 wherein the first silicon oxide layer (SiO2; Figure 4) is deposited on the substrate (Figure 4; "Si wafers" , Section 2.1) by placing the substrate in a process chamber (inherent, "base pressure before sputtering was $2x10^{-7}$ Pa" Section 2.1) applying a sputtering power ("The sputtering power was 4 kW..., Section 2.1, Figure 1a) to reactants to generate a plasma in the process chamber - claim 36.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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